

DATA SHEET

74LVCH32373A

**32-bit transparent D-type latch with
5 V tolerant inputs/outputs; 3-state**

Product specification
File under Integrated Circuits, IC24

1999 Nov 24

32-bit transparent D-type latch with 5 V tolerant inputs/outputs; 3-state

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FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on data inputs
- Typical output ground bounce voltage:
 $V_{OLP} < 0.8 \text{ V}$ at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25 \text{ }^\circ\text{C}$
- Typical output undershoot voltage:
 $V_{OHV} > 2 \text{ V}$ at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25 \text{ }^\circ\text{C}$
- Power off disables outputs, permitting live insertion
- Packaged in plastic fine-pitch ball grid array package.

DESCRIPTION

The 74LVCH32373A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 or 5 V environment.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \text{ }^\circ\text{C}$; $t_r = t_f \leq 2.5 \text{ ns}$.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|---|--|---------|------|
| t_{PHL}/t_{PLH} | propagation delay nD _n to nQ _n | $C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$ | 3.0 | ns |
| | nLE to nQ _n | $C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$ | 3.4 | ns |
| C_I | input capacitance | | 5.0 | pF |
| C_{PD} | power dissipation capacitance per buffer | $V_I = \text{GND to } V_{CC}$; note 1 | 26 | pF |

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

The 74LVCH32373A is a 32-bit transparent D-type latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. One latch enable (nLE) input and one output enable (n $\overline{\text{OE}}$) are provided for each octal. Inputs can be driven from either 3.3 or 5 V devices.

The 74LVCH32373A consists of 4 sections of eight D-type transparent latches with 3-state true outputs. When input nLE is HIGH, data at the nD_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes.

When input nLE is LOW the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of nLE. When input n $\overline{\text{OE}}$ is LOW, the contents of the eight latches are available at the outputs. When input n $\overline{\text{OE}}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the n $\overline{\text{OE}}$ input does not affect the state of the latches.

The 74LVCH32373A bus hold data input circuits eliminate the need for external pull-up resistors to hold unused inputs.

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FUNCTION TABLE

See note 1.

| OPERATING MODE | INPUTS | | | INTERNAL LATCHES | OUTPUTS |
|--|------------------|-----|-----------------|------------------|-----------------|
| | \overline{nOE} | nLE | nD _n | | nQ _n |
| Enable and read register (transparent mode) | L | H | L | L | L |
| | L | H | H | H | H |
| Latch and read register | L | L | l | L | L |
| | L | L | h | H | H |
| Latch register and disable outputs | H | L | l | L | Z |
| | H | L | h | H | Z |

Note

- H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
Z = high-impedance OFF-state.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | | |
|----------------|-------------------|------|---------|----------|----------|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE |
| 74LVCH32373AEC | -40 to +85 °C | 96 | LFBGA96 | plastic | SOT536-1 |

PINNING

| SYMBOL | DESCRIPTION |
|------------------|-----------------------------------|
| nD _n | data inputs |
| nLE | latch enable inputs (active HIGH) |
| nQ _n | data outputs |
| GND | ground (0 V) |
| \overline{nOE} | output enable inputs (active LOW) |
| V _{CC} | DC supply voltage |

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| | | | | | | | | | | | | | | | | |
|---|-------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------|-------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------|
| 6 | 1D ₁ | 1D ₃ | 1D ₅ | 1D ₇ | 2D ₁ | 2D ₃ | 2D ₅ | 2D ₇ | 3D ₁ | 3D ₃ | 3D ₅ | 3D ₇ | 4D ₁ | 4D ₃ | 4D ₅ | 4D ₆ |
| 5 | 1D ₀ | 1D ₂ | 1D ₄ | 1D ₆ | 2D ₀ | 2D ₂ | 2D ₄ | 2D ₆ | 3D ₀ | 3D ₂ | 3D ₄ | 3D ₆ | 4D ₀ | 4D ₂ | 4D ₄ | 4D ₇ |
| 4 | 1LE | GND | V _{CC} | GND | GND | V _{CC} | GND | 2LE | 3LE | GND | V _{CC} | GND | GND | V _{CC} | GND | 4LE |
| 3 | 1 \overline{OE} | GND | V _{CC} | GND | GND | V _{CC} | GND | 2 \overline{OE} | 3 \overline{OE} | GND | V _{CC} | GND | GND | V _{CC} | GND | 4 \overline{OE} |
| 2 | 1Q ₀ | 1Q ₂ | 1Q ₄ | 1Q ₆ | 2Q ₀ | 2Q ₂ | 2Q ₄ | 2Q ₆ | 3Q ₀ | 3Q ₂ | 3Q ₄ | 3Q ₆ | 4Q ₀ | 4Q ₂ | 4Q ₄ | 4Q ₇ |
| 1 | 1Q ₁ | 1Q ₃ | 1Q ₅ | 1Q ₇ | 2Q ₁ | 2Q ₃ | 2Q ₅ | 2Q ₇ | 3Q ₁ | 3Q ₃ | 3Q ₅ | 3Q ₇ | 4Q ₁ | 4Q ₃ | 4Q ₅ | 4Q ₆ |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |

Fig.1 Pin configuration.

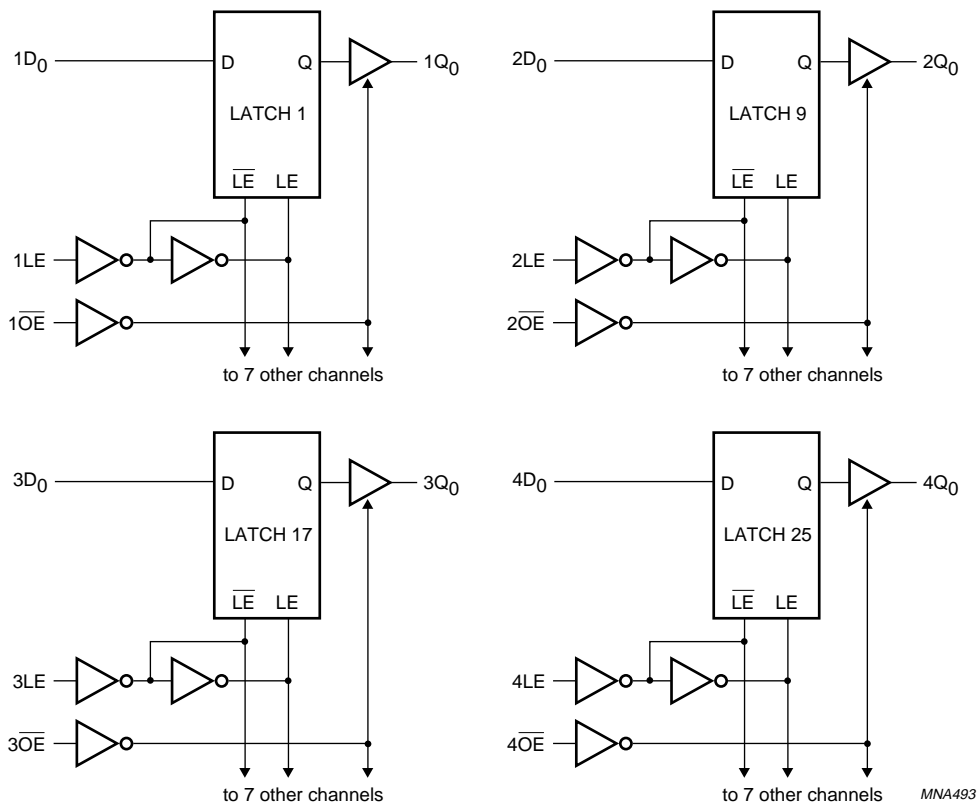


Fig.2 Logic symbol.

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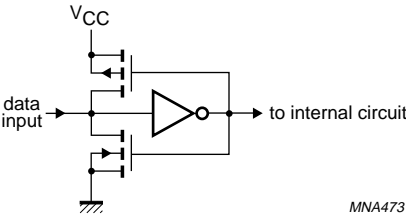


Fig.3 Bus hold circuit.

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|---|-------------------------------|--|--------|-----------------|------|
| | | | MIN. | MAX. | |
| V _{CC} | DC supply voltage | maximum speed performance | 2.7 | 3.6 | V |
| | | low-voltage applications | 1.2 | 3.6 | V |
| V _I | DC input voltage | | 0 | 5.5 | V |
| V _O | DC output voltage | HIGH or LOW state | 0 | V _{CC} | V |
| | | 3-state | 0 | 5.5 | V |
| T _{amb} | operating ambient temperature | see DC and AC characteristics per device | -40 | +85 | °C |
| t _r , t _f (Δt/Δf) | input rise and fall times | V _{CC} = 1.2 to 2.7 V | 0 | 20 | ns/V |
| | | V _{CC} = 2.7 to 3.6 V | 0 | 10 | |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------------------------|-----------------------------------|--|------|-----------------------|------|
| V _{CC} | DC supply voltage | | -0.5 | +6.5 | V |
| V _I | DC input voltage | note 1 | -0.5 | +6.5 | V |
| I _{IK} | DC input diode current | V _I < 0 | - | -50 | mA |
| I _{OK} | DC output diode current | V _O > V _{CC} or V _O < 0; note 1 | - | ±50 | mA |
| V _O | DC output voltage | HIGH or LOW state; note 1 | -0.5 | V _{CC} + 0.5 | V |
| | | 3-state; note 1 | -0.5 | +6.5 | V |
| I _O | DC output source or sink current | V _O = 0 to V _{CC} | - | ±50 | mA |
| I _{CC} , I _{GND} | DC V _{CC} or GND current | | - | ±100 | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _D | power dissipation per package | temperature range -40 to +85 °C; note 2 | - | 1000 | mW |

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 70 °C the value of P_D derates linearly with 1.8 mW/K.

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DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | $T_{amb} -40 \text{ to } +85^{\circ}\text{C}$ | | | UNIT |
|-----------------|---|--|--------------------|---|---------------------|----------|---------------|
| | | OTHER | $V_{CC}(\text{V})$ | MIN. | TYP. ⁽¹⁾ | MAX. | |
| V_{IH} | HIGH-level input voltage | | 1.2 | V_{CC} | – | – | V |
| | | | 2.7 to 3.6 | 2.0 | – | – | |
| V_{IL} | LOW-level input voltage | | 1.2 | – | – | GND | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | 2.7 | $V_{CC} - 0.5$ | – | – | V |
| | | $I_O = -12 \text{ mA}$ | 3.0 | $V_{CC} - 0.2$ | V_{CC} | – | |
| | | $I_O = -100 \mu\text{A}$ | 3.0 | $V_{CC} - 0.6$ | – | – | |
| | | $I_O = -18 \text{ mA}$ | 3.0 | $V_{CC} - 0.8$ | – | – | |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | 2.7 | – | – | 0.40 | V |
| | | $I_O = 12 \text{ mA}$ | 3.0 | – | – | 0.20 | |
| | | $I_O = 100 \mu\text{A}$ | 3.0 | – | – | 0.55 | |
| | | $I_O = 24 \text{ mA}$ | 3.0 | – | – | 0.55 | |
| I_I | input leakage current | $V_I = 5.5 \text{ V}$ or GND; note 2 | 3.6 | – | ± 0.1 | ± 5 | μA |
| I_{OZ} | 3-state output OFF-state current | $V_I = V_{IH}$ or V_{IL} ; $V_O = 5.5 \text{ V}$ or GND | 3.6 | – | 0.1 | ± 5 | μA |
| I_{off} | power off leakage supply current | V_I or $V_O = 5.5 \text{ V}$ | 0.0 | – | 0.1 | ± 10 | μA |
| I_{CC} | quiescent supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ | 3.6 | – | 0.1 | 40 | μA |
| ΔI_{CC} | additional quiescent supply current per input pin | $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0$ | 2.7 to 3.6 | – | 5 | 500 | μA |
| I_{BHL} | bus hold LOW sustaining current | $V_I = 0.8 \text{ V}$; notes 3, 4 and 5 | 3.0 | 75 | – | – | μA |
| I_{BHH} | bus hold HIGH sustaining current | $V_I = 2.0 \text{ V}$; notes 3, 4 and 5 | 3.0 | –75 | – | – | μA |
| I_{BHLO} | bus hold LOW overdrive current | notes 3, 4 and 6 | 3.6 | 500 | – | – | μA |
| I_{BHHO} | bus hold HIGH overdrive current | notes 3, 4 and 6 | 3.6 | –500 | – | – | μA |

Notes

1. All typical values are at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25^{\circ}\text{C}$.
2. For bus hold parts the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5 V on the input terminal.
3. Valid for data inputs of bus hold parts (LVCH32-A) only.
4. For data inputs only; control inputs do not have a bus hold circuit.
5. The specified sustaining current at the data input holds the input below the specified V_I level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input level.

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AC CHARACTERISTICS

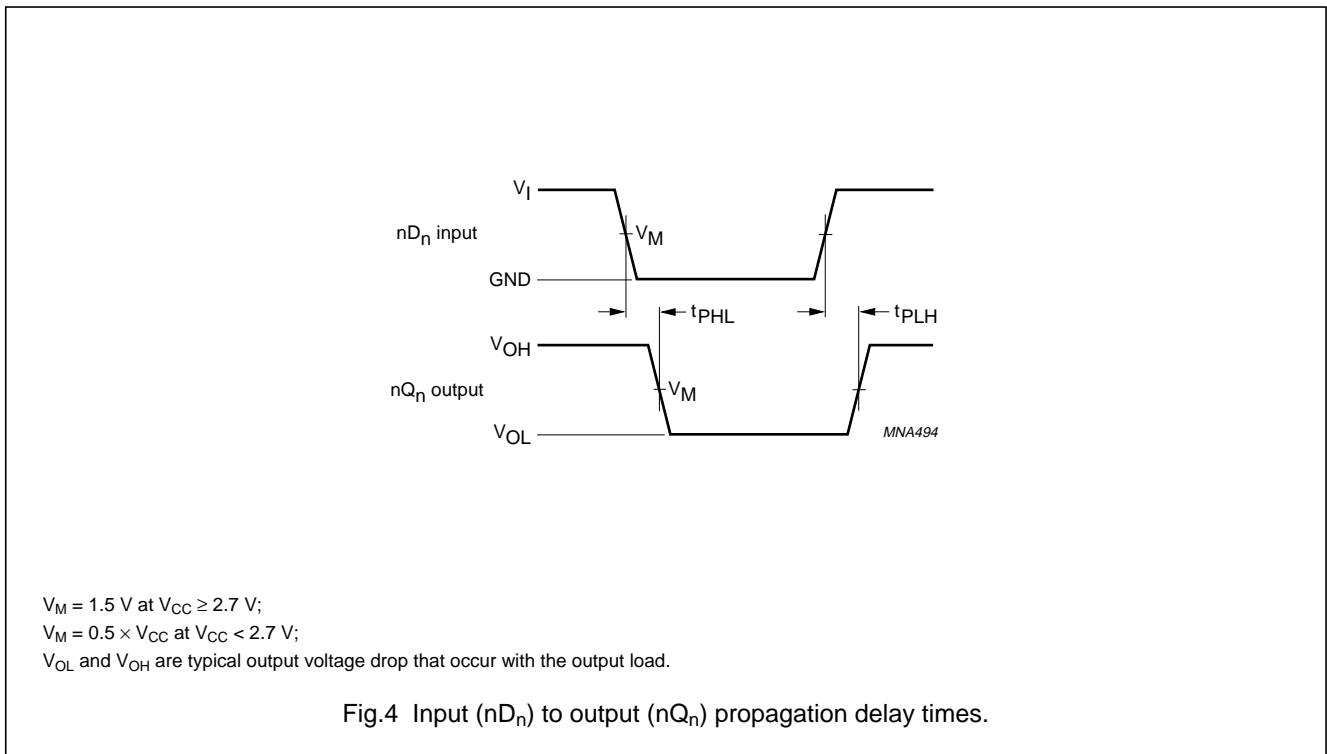
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500 \Omega$.

| SYMBOL | PARAMETER | TEST CONDITIONS | | $T_{amb} = -40$ to $+85$ °C | | | UNIT |
|-------------------|--|------------------|--------------|-----------------------------|---------------------|------|------|
| | | WAVEFORMS | V_{CC} (V) | MIN. | TYP. ⁽¹⁾ | MAX. | |
| t_{PHL}/t_{PLH} | propagation delay nD_n to nQ_n | see Figs 4 and 8 | 2.7 | 1.5 | – | 5.7 | ns |
| | | | 3.0 to 3.6 | 1.5 | 3.0 | 4.7 | |
| t_{PHZ}/t_{PZL} | 3-state output enable time nOE to nQ_n | see Figs 7 and 8 | 2.7 | 1.5 | – | 6.5 | ns |
| | | | 3.0 to 3.6 | 1.5 | 3.5 | 5.5 | |
| t_{PHZ}/t_{PLZ} | 3-state output disable time nOE to nQ_n | see Figs 7 and 8 | 2.7 | 1.5 | – | 6.4 | ns |
| | | | 3.0 to 3.6 | 1.5 | 3.9 | 5.4 | |
| t_W | nLE pulse width HIGH | see Figs 5 and 8 | 2.7 | 3.0 | – | – | ns |
| | | | 3.0 to 3.6 | 3.0 | 2.0 | – | |
| t_{su} | set-up time nD_n to nLE | see Figs 6 and 8 | 2.7 | 1.7 | – | – | ns |
| | | | 3.0 to 3.6 | +1.7 | –0.1 | – | |
| t_h | hold time nD_n to nLE | see Figs 6 and 8 | 2.7 | 1.2 | – | – | ns |
| | | | 3.0 to 3.6 | 1.2 | 0.1 | – | |

Note

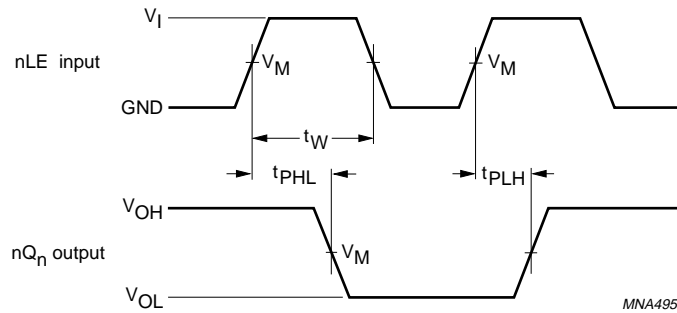
1. All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

AC WAVEFORMS



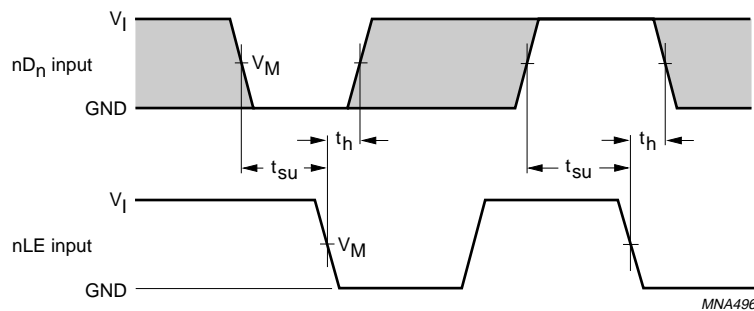
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$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$;
 V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 Latch enable inputs (nLE) pulse width and the latch enable input to outputs (nQn) propagation delay times.

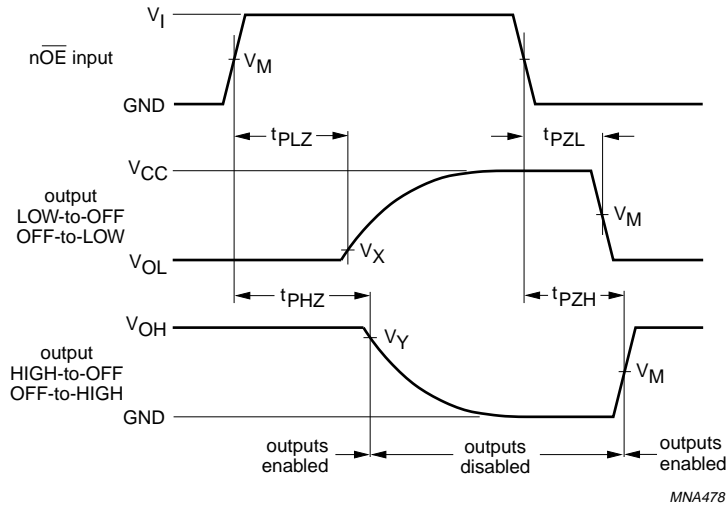


$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$.

Fig.6 Set-up and hold times for inputs (nDn) to inputs (nLE).

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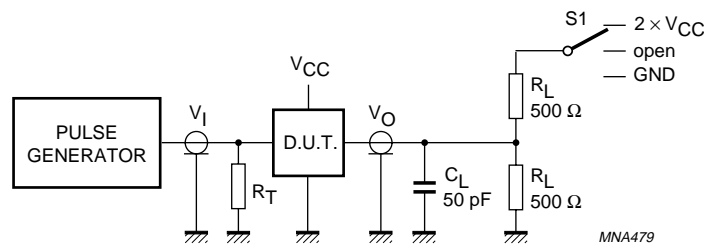
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$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$;
 $V_X = V_{OL} + 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_X = V_{OL} + 0.1\text{ V}$ at $V_{CC} < 2.7\text{ V}$;

$V_Y = V_{OH} - 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_Y = V_{OH} - 0.1\text{ V}$ at $V_{CC} < 2.7\text{ V}$;
 V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 3-state output enable and disable times.



| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | V_I |
|------------------------------|----------------|
| $< 2.7\text{ V}$ | V_{CC} |
| $2.7\text{ to }3.6\text{ V}$ | 2.7 V |

Definitions for test circuit:
 R_L = load resistor.
 C_L = load capacitance including jig and probe capacitance.
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

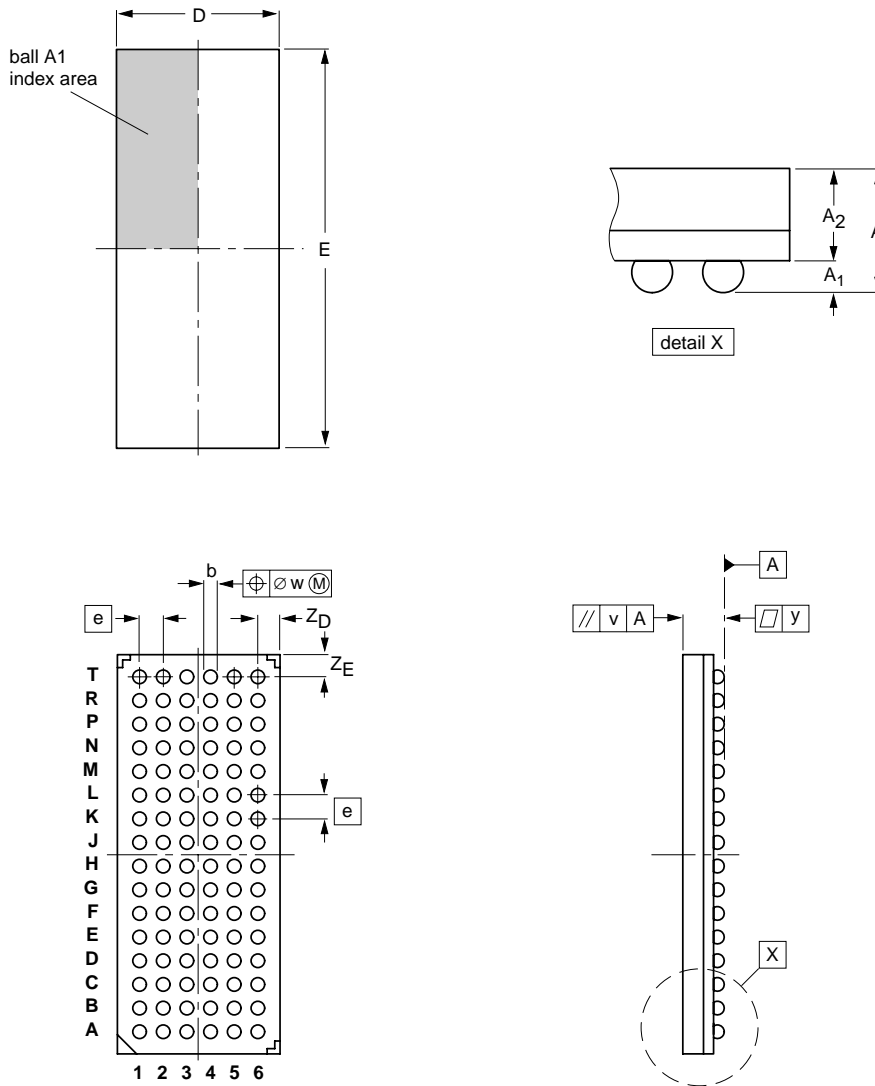
Fig.8 Load circuitry for switching times.

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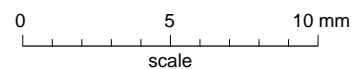
PACKAGE OUTLINE

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | b | D | E | e | v | w | y | Z _D | Z _E |
|------|--------|----------------|----------------|--------------|------------|--------------|-----|-----|------|-----|----------------|----------------|
| mm | 1.5 | 0.41 0.31 | 1.2 0.9 | 0.51 0.41 | 5.6 5.4 | 13.6 13.4 | 0.8 | 0.2 | 0.15 | 0.1 | 0.93 0.58 | 0.93 0.58 |



| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT536-1 | | | | | | 98-11-25 99-06-03 |

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|--|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽¹⁾ |
| BGA, LFBGA, SQFP, TFBGA | not suitable | suitable |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS | not suitable ⁽²⁾ | suitable |
| PLCC ⁽³⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽³⁾⁽⁴⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁵⁾ | suitable |

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

LIFE SUPPORT APPLICATIONS

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NOTES

32-bit transparent D-type latch with
5 V tolerant inputs/outputs; 3-state

74LVCH32373A

NOTES

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